HERMETIC PACKAGES AND FEEDTHROUGHS FOR NEURAL PROSTHESES

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Center For Integrated Microsystems
Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, Michigan 48109-2122

Program Personnel:

Faculty:
Professor Khalil Najafi: Principal Investigator
Professor David J. Anderson: Biological Experiments

Staff:
Mr. James Wiler: Animal Implants and Surgery

Graduate Student Research Assistants:
Mr. Timothy Harpster: Package Fabrication and Telemetry Testing
Mr. Rajagopalan Rangarajan: FINESS Chip
Mr. Brian Stark: Packaging and Accelerated Testing

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SUMMARY

During the past quarter, we continued testing and characterization of the wireless humidity monitoring system and monitored the hermeticity of these packages in animal hosts. We made advances in thick coil electroplating and continued to develop alternative methods for biocompatible packaging. We optimized the transmitter for transmitting adequate power to the FINESS chip.

Four glass-silicon packages have been soaking on PBS at room temperatures. As of the end of this quarter, all these packages are still intact and the longest package has been soaking for a total of 1951 days. These packages will continue their soak test until failure is detected.

A wireless system that consists of a hybrid coil and a polyimide relative humidity sensor has been developed. We have packaged a wireless system and soaked in high temperature saline and after 12 months in saline at 97°C, the humidity monitoring system is functional and the package is still dry (confirmed with visual inspection). Six glass-silicon packages with HMS systems have been implanted into various locations in two guinea pigs and after 11 months they all indicate that the packages are hermetic and intact.

Many advances have been made in thick resist processing, copper electroplating and FI-HMS (Fully Integrated Humidity Monitoring System) fabrication. A 30μm thick resist process has been developed whereas previous processes have used a 20μm resist process. A new copper electroplating process has improved uniformity, plating rate, and resistivity of electroplated copper. Devices have been fabricated with sensitivities ranging from 7.56-16.6 kHz per %RH which is an improvement over the hybrid design of 5-8kHz per %RH.

We have continued to develop alternative methods for biocompatible packaging. We have further investigated localized heating and made significant improvements in the heater structure to improve this packaging technology.

We developed a new transmitter for powering the FINESS chips. This transmitter was tested with the hybrid coils and found to transmit sufficient power. We also developed some equations for predicting the power transfer in the FINESS chip-transmitter system better.

I. INTRODUCTION

This project aims at the development of hermetic, biocompatible micropackages and feedthroughs for use in a variety of implantable neural prostheses for sensory and motor handicapped individuals. In addition, it will also develop a telemetry system for monitoring package humidity in unrestrained animals, and of telemetry electronics and packaging for stimulation of peripheral nerves. The primary objectives of the proposed research are: 1) the development and characterization of hermetic packages for miniature, silicon-based, implantable neural prostheses designed to interface with the nervous system for many decades; 2) the development of techniques for providing multiple sealed feedthroughs for the hermetic package; 3) the development of custom-designed packages and systems used in several different chronic stimulation or recording applications in the central or peripheral nervous systems in collaboration and cooperation with groups actively involved in developing such systems; and 4) establishing the functionality and biocompatibility of these custom-designed packages in *in-vivo* applications. Although the proposed research is focused on the development of the package and feedthroughs, it also aims at the development of inductively powered systems that can be used in many implantable recording and stimulation devices in general, and of multichannel microstimulators for functional neuromuscular stimulation, and multichannel recording microprobes for CNS applications in particular.

Our group here at the Center for Integrated Sensors and Circuits at the University of Michigan has been involved in the development of silicon-based multichannel recording and stimulating microprobes for use in the central and peripheral nervous systems. More specifically, during the past three contract periods dealing with the development of a single-channel inductively powered microstimulator, our research and development program has made considerable progress in a number of areas related to the above goals. A hermetic packaging technique based on electrostatic bonding of a custom-made glass capsule and a supporting silicon substrate has been developed and has been shown to be hermetic for a period of at least a few decades in salt water environments. This technique allows the transfer of multiple interconnect leads between electronic circuitry and hybrid components located in the sealed interior of the capsule and electrodes located outside of the capsule. The glass capsule can be fabricated using a variety of materials and can be made to have arbitrary dimensions as small as 1.8mm in diameter. A multiple sealed feedthrough technology has been developed that allows the transfer of electrical signals through polysilicon conductor lines located on a silicon support substrate. Many feedthroughs can be fabricated in a small area. The packaging and feedthrough techniques utilize biocompatible materials and can be integrated with a variety of micromachined silicon structures.

The general requirements of the hermetic packages and feedthroughs to be developed under this project are summarized in Table 1. Under this project we will concentrate our efforts to satisfy these requirements and to achieve the goals outlined above. There are a variety of neural prostheses used in different applications, each having different requirements for the package, the feedthroughs, and the particular system application. The overall goal of the program is to develop a miniature hermetic package that can seal a variety of electronic components such as capacitors and coils, and integrated circuits and sensors (in particular electrodes) used in neural prostheses. Although the applications are different, it is possible to

identify a number of common requirements in all of these applications in addition to those requirements listed in Table 1. The packaging and feedthrough technology should be capable of:

1- protecting non-planar electronic components such as capacitors and coils, which typically have large dimensions of about a few millimeters, without damaging them;
2- protecting circuit chips that are either integrated monolithically or attached in a hybrid fashion with the substrate that supports the sensors used in the implant;
3- interfacing with structures that contain either thin-film silicon microelectrodes or conventional microelectrodes that are attached to the structure;

Table 1: General Requirements for Miniature Hermetic Packages and Feedthroughs for Neural Prostheses Applications.

Package Lifetime:
≥ 40 Years in Biological Environments @ 37°C

Packaging Temperature:
≤360°C

Package Volume:
10-100 cubic millimeters

Package Material:
Biocompatible
Transparent to Light
Transparent to RF Signals

Package Technology:
Batch Manufactureable

Package Testability:
Capable of Remote Monitoring
In-Situ Sensors (Humidity & Others)

Feedthroughs:
At Least 12 with ≤125μm Pitch
Compatible with Integrated or Hybrid Microelectrodes
Sealed Against Leakage

Testing Protocols:
In-Vitro Under Accelerated Conditions
In-Vivo in Chronic Recording/Stimulation Applications

We have identified two general categories of packages that need to be developed for implantable neural prostheses. The first deals with those systems that contain large components like capacitors, coils, and perhaps hybrid integrated circuit chips. The second deals with those systems that contain only integrated circuit chips that are either integrated in the substrate or are attached in a hybrid fashion to the system.

Figure 1 shows our general proposed approach for the package required in the first category. This figure shows top and cross-sectional views of our proposed approach here. The package is a glass capsule that is electrostatically sealed to a support silicon substrate. Inside the glass capsule are housed all of the necessary components for the system. The electronic circuitry needed for any analog or digital circuit functions is either fabricated on a separate circuit chip that is hybrid mounted on the silicon substrate and electrically connected to the silicon substrate, or integrated monolithically in the support silicon substrate itself. The attachment of the hybrid IC chip to the silicon substrate can be performed using a number of different technologies such as simple wire bonding between pads located on each substrate, or using more sophisticated techniques such as flip-chip solder reflow or tab bonding. The larger capacitor or microcoil components are mounted on either the substrate or the IC chip using appropriate epoxies or solders. This completes the assembly of the electronic components of the system and it should be possible to test the system electronically at this point before the package is completed. After testing, the system is packaged by placing the glass capsule over the entire system and bonding it to the silicon substrate using an electrostatic sealing process. The cavity inside the glass package is now hermetically sealed against the outside environment. Feedthroughs to the outside world are provided using the grid-feedthrough technique discussed in previous reports. These feedthroughs transfer the electrical signals between the electronics inside the package and various elements outside of the package. If the package has to interface with conventional microelectrodes, these microelectrodes can be attached to bonding pads located outside of the package; the bond junctions will have to be protected from the external environment using various polymeric encapsulants. If the package has to interface with on-chip electrodes, it can do so by integrating the electrode on the silicon support substrate. Interconnection is simply achieved using on-chip polysilicon conductors that make the feedthroughs themselves. If the package has to interface with remotely located recording or stimulating electrodes that are attached to the package using a silicon ribbon cable, it can do so by integrating the cable and the electrodes again with the silicon support substrate that houses the package and the electronic components within it.

Figure 2 shows our proposed approach to package development for the second category of applications. In these applications, there are no large components such as capacitors and coils. The only component that needs to be hermetically protected is the electronic circuitry. This circuitry is either monolithically fabricated in the silicon substrate that supports the electrodes (similar to the active multichannel probes being developed by the Michigan group), or is hybrid attached to the silicon substrate that supports the electrodes (like the passive probes being developed by the Michigan group). In both of these cases the package is again another glass capsule that is electrostatically sealed to the silicon substrate. Notice that in this case, the glass package need not be a high profile capsule, but rather it need only have a cavity that is deep enough to allow for the silicon chip to reside within it. Note that although the silicon IC chip is originally 500μm thick, it can be thinned down to about 100μm, or can be recessed in a cavity created in the silicon substrate itself. In either case, the recess in the glass is less than 100μm

deep (as opposed to several millimeters for the glass capsule). Such a glass package can be easily fabricated in a batch process from a larger glass wafer.

The above two approaches address the needs for most implantable neural prostheses. Note that both of these techniques utilize a silicon substrate as the supporting base, and are not directly applicable to structures that use other materials such as ceramics or metals. Although this may seem a limitation at first, we believe that the use of silicon is, in fact, an advantage because it is biocompatible and many emerging systems use silicon as a support substrate.

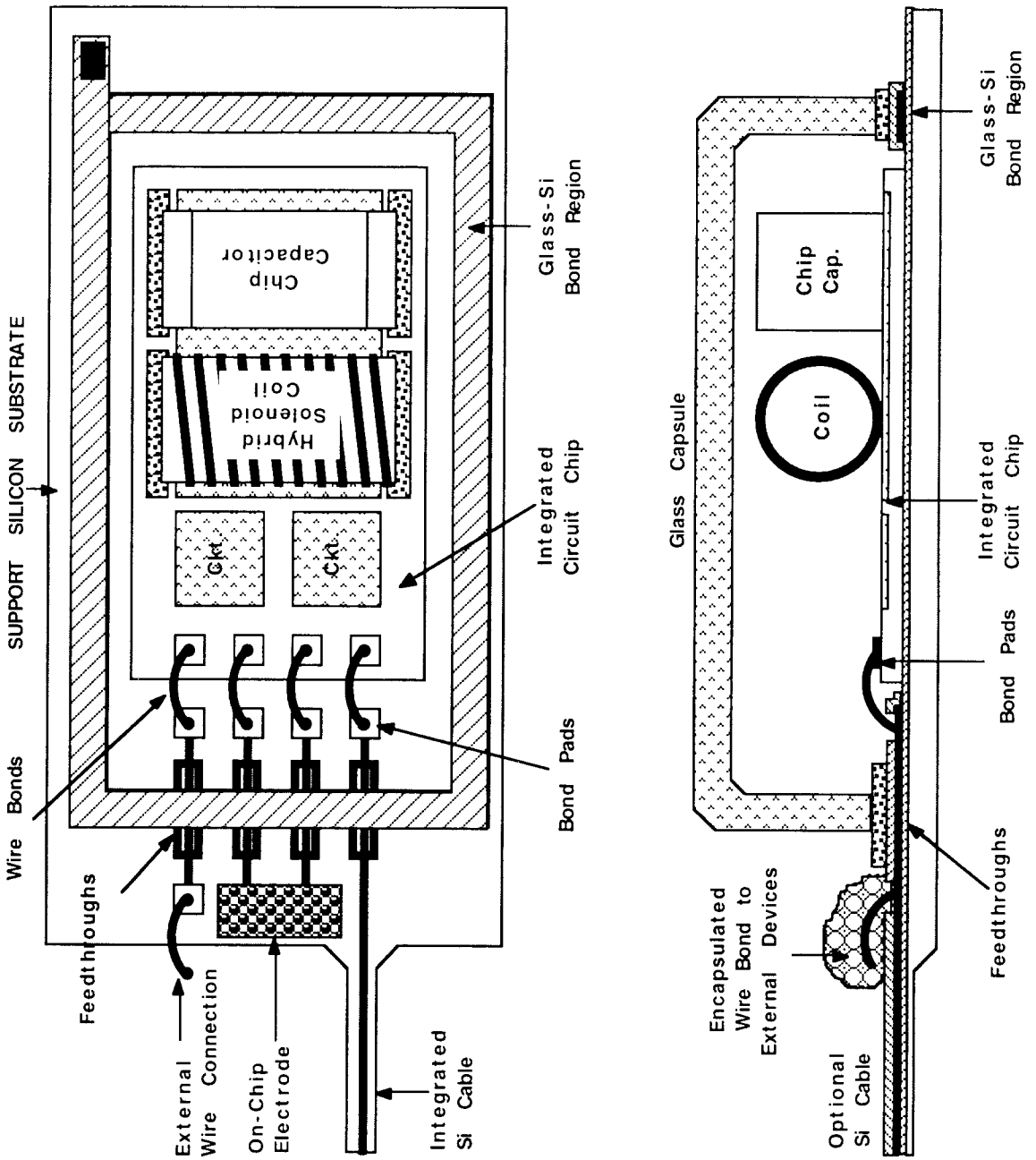


Figure 1: A generic approach for packaging implantable neural prostheses that contain a variety of components such as chip capacitors, microcoils, and integrated circuit chips. This packaging approach allows for connecting to a variety of electrodes.

We will further improve the silicon glass package and its built-in feedthroughs, and will study and explore alternative technologies for hermetic packaging of implantable systems. In particular, we have proposed using a silicon capsule that can be electrostatically bonded to a silicon substrate thus allowing the capsule to be machined down to dimensions below a 100μm. We will also develop an implantable telemetry system for monitoring package humidity in unrestrained animals for a period of at least one year. Two separate systems have been proposed, one based on a simple oscillator, and the other based on a switched-capacitor readout interface circuit and an on-chip low-power AD converter, both using a polyimide-based humidity sensor. This second system will telemeter the humidity information to an outside receiver using a 300MHz on-chip transmitter.

Finally, we have forged potential collaborations with two groups working in the development of recording/stimulating systems for neural prostheses. The first group is that led by Professor Ken Wise at the University of Michigan, which has been involved in the development of miniature, silicon-based multichannel recording and stimulation system for the CNS for many years. Through this collaboration we intend to develop hermetic packages and feedthroughs for a 3-D recording/stimulation system that is under development at Michigan. We will also develop the telemetry front end necessary to deliver power and data to this system. The second group is at Case Western Reserve University, led by Prof. D. Durand, and has been involved in recording and stimulation from peripheral nerves using cuff electrodes. Through this collaboration we intend to develop a fully integrated, low profile, multichannel, hermetic, wireless peripheral nerve stimulator that can be used with their nerve cuff electrode. This system can be directly used with other nerve cuffs that a number of other groups around the country have developed. Both of these collaborations should provide us with significant data on the reliability and biocompatibility of the package.

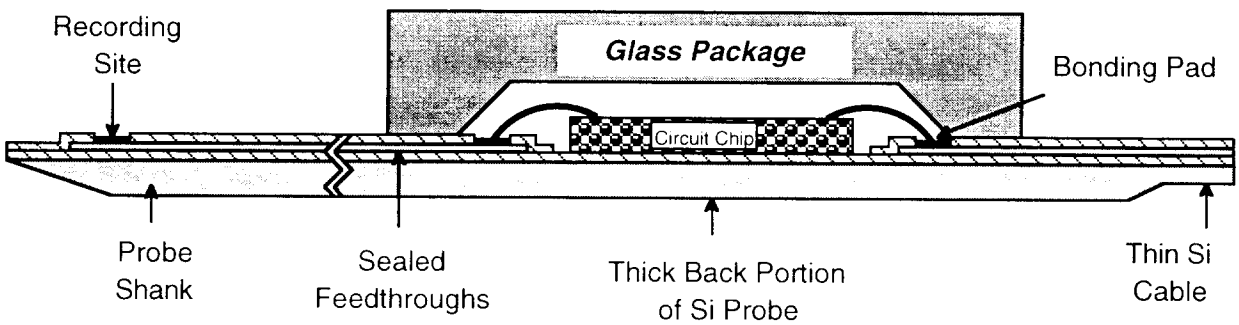


Figure 2: Proposed packaging approach for implantable neural prostheses that contain electronic circuitry, either monolithically fabricated in the probe substrate or hybrid attached to the silicon substrate containing microelectrodes.

II. ACTIVITIES DURING THE PAST QUARTER

2.1 Hermetic Packaging

Over the past few years we have developed a biocompatible hermetic package with high density multiple feedthroughs. This technology utilizes electrostatic bonding of a custom-made glass capsule to a silicon substrate to form a hermetically sealed cavity, as shown in Figure 3. Feedthrough lines are obtained by forming closely spaced polysilicon lines and planarizing them with LTO and PSG. The PSG is reflowed in steam at 1100°C for 2 hours to form a planarized surface. A passivation layer of oxide/nitride/oxide is then deposited on top to prevent direct exposure of PSG to moisture. A layer of fine-grain polysilicon (surface roughness 50Å rms) is deposited and doped to act as the bonding surface. Finally, a glass capsule is bonded to this top polysilicon layer by applying a voltage of 2000V between the two for 12 minutes at 320 to 350°C, a temperature compatible with most hybrid components. The glass capsule can be either custom molded from Corning code #7740 glass, or can be batch fabricated using ultrasonic micromachining of #7740 glass wafers.

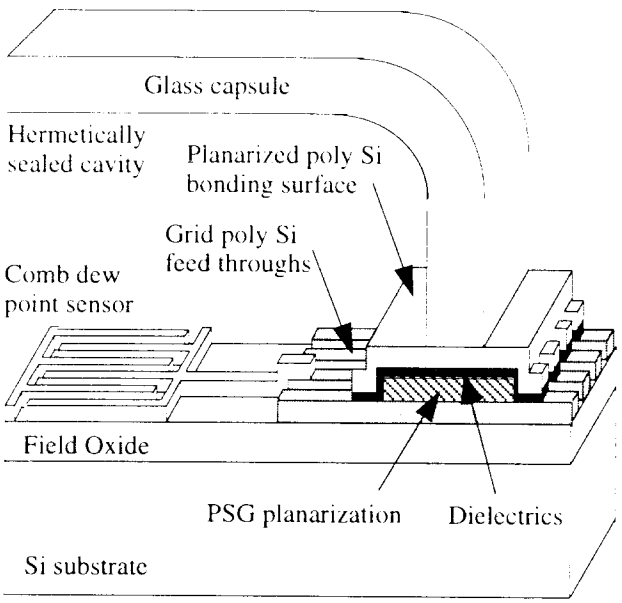


Figure 3: The structure of the hermetic package with grid feedthroughs.

During the past few years we have electrostatically bonded and soak tested over one hundred and sixty of these packages. The bonding yield is about 82% (yield is defined as the percentage of packages which last more than 24 hours in the solution they are soaked in). At the beginning of this quarter 4 devices were still being tested in saline at room temperature. These devices have been under test for over 5 years and show no sign of leakage. We should mention that these devices have been made with silicon substrates that are thinned (~150μm) and bonded to the custom molded glass capsules. We have also continued fabrication of silicon substrates and also continued several in-vivo tests using a wireless humidity sensor-hybrid coil system.

2.1.1 Ongoing Room Temperature Soak Tests in Saline

The packages soaked in phosphate buffered saline at room temperature have been under test for over 5 years. These soak tests were started to complement the accelerated soak tests at the higher temperatures. Furthermore, upon close inspection of the top polysilicon layer, it is found that this top layer is there and is not etched after nearly 5 years of testing. Our conclusion is that at room temperature we are below the activation energy required to cause dissolution of polysilicon and hence we have not yet observed any dissolution related failures. This observation is in accordance with the acceleration model used in interpreting the high temperature tests. Indeed, it seems to confirm that the activation energy for the dissolution of the substrate or the top polysilicon is high. Accordingly, due to the exponential decrease of the acceleration factor with temperature, the dissolution of silicon or polysilicon may not be significant at the body temperature.

Out of the original 6 packages, one failed prematurely the first day and one failed because of mishandling. The 4 other devices are still under test and present no sign of leakage into the capsule after being soaked for 1951 days. Table 2 summarizes the data obtained from these soak tests.

Table 2: Data for room temperature soak tests in saline.

Number of packages in this study	6
Soaking solution	Saline
Failed within 24 hours (not included in MTTF)	1
Packages lost due to mishandling	1
Longest lasting packages in this study	1951 days
Packages still under tests with no measurable room temperature condensation inside	4
Average lifetime to date (MTTF) so far including losses due to mishandling	1586 days
Average lifetime to date (MTTF) so far excluding losses due to mishandling	1942 days

2.2 Wireless Monitoring of Humidity Inside Glass-Silicon Packages

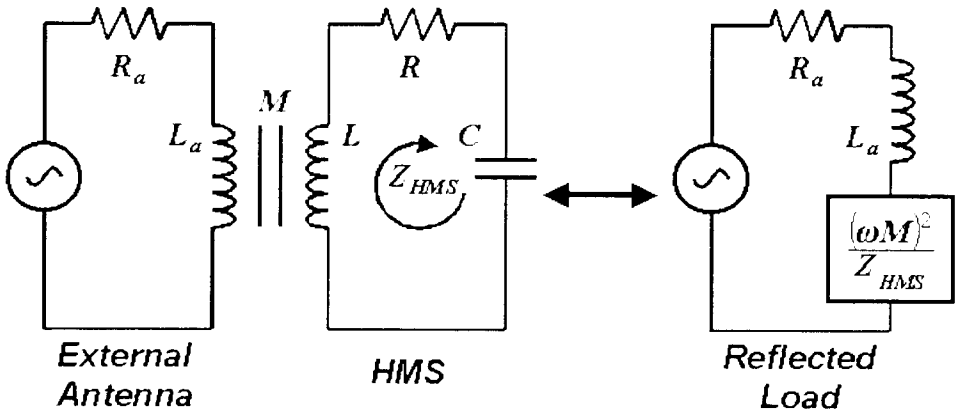
A wireless humidity monitoring system (HMS) has several benefits. First, it greatly facilitates the in-vitro testing of the packages, decreasing the detection threshold of moisture (as compared to dew point sensors used in the room temperature saline tests) and reducing mishandling and temperature cycling. In addition, it would allow one to automate the in-vitro testing procedure. Another benefit is that it allows continuous monitoring of humidity in packages that are implanted in animal hosts, thus providing important in-vivo hermeticity data.

In the previous quarterly reports, the wireless humidity monitoring approach was explained, which can be summarized as the following: a capacitive polyimide humidity sensor (HS) is wire bonded to an inductor made by copper wires wound around a ferrite core. This coil with the HS forms a LC tank circuit. The capacitive humidity sensor in this tank circuit responds to changes in humidity by changing its capacitance and thus the resonance frequency of the tank circuit shifts. When a coil (external antenna) is placed nearby this tank circuit, the maximum loading in the impedance measurements of the antenna is observed at the resonance frequency of the tank circuit allowing one to remotely monitor changes in humidity levels. We thus call the HS and the inductor combination the Humidity Monitoring System (HMS).

2.2.1 System Configuration

The wireless monitoring system consists of an external loop antenna (of inductance L_a), inductively coupled to the humidity monitoring system (HMS). The HMS is a hybrid copper wire coil (with inductance L and series resistance R) wire bonded to a humidity sensor (with capacitance C varying with humidity). The hybrid coil inside the package is modeled as a solenoid (a valid approximation, however, the actual coil has a rectangular shape) and for simplicity, we assume that the antenna coil and the HMS coil are coaxial.

The schematic of the system is given in Figure 4 and the equation nomenclature for this system is given in Table 3.



(a) System configuration (b) Equivalent circuit

Figure 4: The schematic of the humidity monitoring system.

Table 3: Equation nomenclature for the HMS.

Antenna:	Humidity Monitoring System:
L_a self-inductance (H)	L coil self-inductance (H)
a radius (m)	d coil diameter (m)
N_a number of turns	l coil length (m)
μ_o permeability (4πe-7 Ohms/m)	S cross sectional area (m^2)
	$\mu=\mu_o\mu_r$ magnetic permeability
Coupling:	μ_r relative permeability of the core
M mutual inductance	C capacitance of the humidity sensor
Z axis distance	R series resistance

Figure 5 shows a HMS used to test the hermeticity of glass-Si anodic bonding. Figure 6 shows the antenna testing setup with a half diced glass capsule revealing the HMS inside.

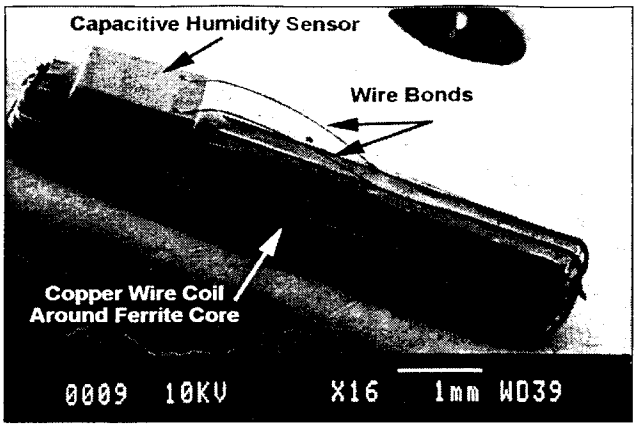


Figure 5: An assembled HMS.

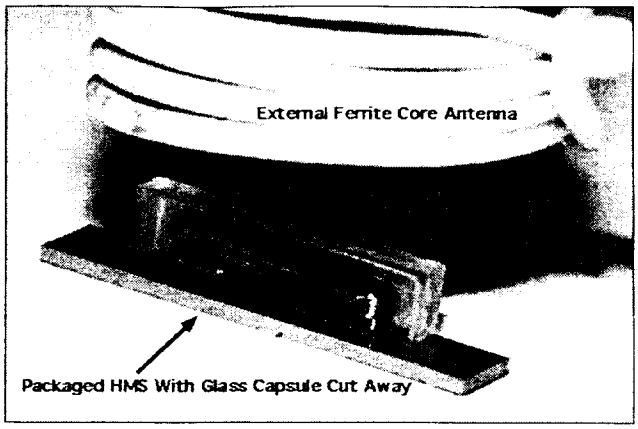


Figure 6: External Antenna and half-diced glass with enclosed HMS.

A technical paper entitled "A Passive Humidity Monitoring System For In-Situ Remote Wireless Testing Of Micropackages" describing the HMS and wireless telemetry monitoring was presented at the MEMS 2000 conference in Miyazaki, Japan [5].

2.2.2 High Temperature Soak Test in Saline

An anodically sealed Humidity Monitoring System (HMS) has been soaking since April 1999 in phosphate buffered saline solution at high temperature. The package is inspected routinely under a microscope to detect any leakage path(s) on the bonding surface, and the resonant frequency of the HMS is measured to correlate this response with the humidity inside the sealed package. This data may provide useful information as to the failure and degradation processes of the package hermeticity. As of mid April 2000, neither a complete leakage path nor a corresponding HMS resonant frequency shift has been observed. Figure 7 shows the percent relative humidity change versus the number of days soaking at 97°C.

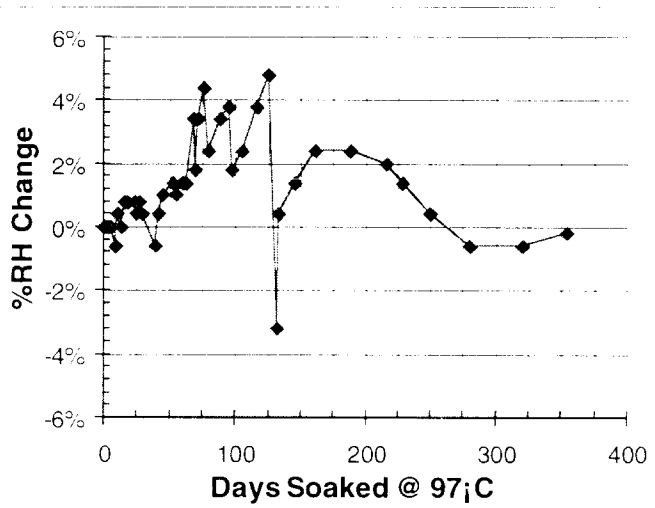


Figure 7: Telemetry data from a package soaked in high-temperature saline soak test (97°C).

The frequency variations are attributed to day to day temperature fluctuations during testing. These variations are within experimental error and hence the HMS data and visual inspection analysis strongly suggest the anodically sealed package is hermetic after 1 year.

2.3 A New Fully Integrated Humidity Monitoring System

A new Fully Integrated Humidity Monitoring System (FI-HMS) is being developed to address the deficiencies of the HMS discussed in the September 1999 NIH report and summarized in Table 4.

Table 4: Deficiencies of the hybrid HMS design

– Tedious time consuming fabrication – Multiple component system – low yield – Variation of performance due to hand assembly – Large device size

The new design is shown in Figure 8 and is applicable to the same wireless testing model described in section 2.2.1.

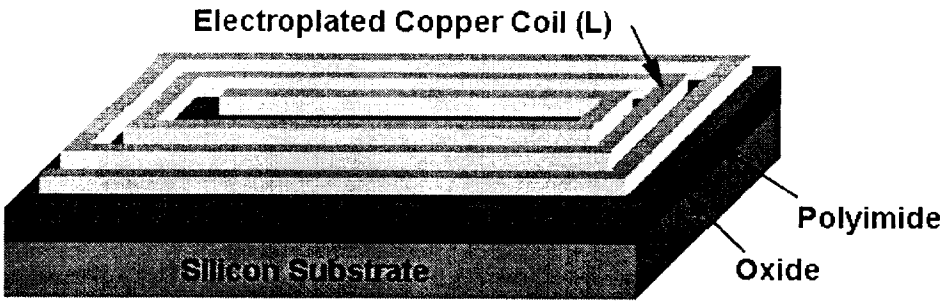


Figure 8: A Fully-Integrated-HMS design.

The equivalent circuit of this design is an LC tank circuit as shown in Figure 4 where the inductor, with inductance L and series resistance R, is the planar copper coil and the capacitor, with capacitance C, is between the copper coil and the conductive silicon substrate separated by dielectrics (in this case – SiO_2 and humidity sensitive polyimide).

Many advancements have been made this quarter in the development of the FI-HMS system. New thick resist processes have been explored and a 30μm thick resist (as opposed to the well established 20μm resist process) has been used for plating FI-HMS coils and may contribute to other wireless devices such as the coils used for receiving power and data for the FINESS chips. A new copper electroplating process is used which plates a more uniform and higher quality copper than the electroplating process used for the past couple years at the university and will contribute to this and other projects. Also, initial FI-HMS data shows a greater kHz shift per %RH which implies greater sensitivity to that of the hybrid HMS. These advancements are discussed in detail in the following sections.

2.3.1 Advancements in Thick Resist Processing

The advantage of electroplating thicker coils is to reduce the series resistance and thereby increase the Q of the coil. Two results of reduced FI-HMS coil resistance is 1) a greater Q for accurate resonant frequency measurements and thus accurate %RH measurements, and 2) a greater testing distance because the magnitude of the phase dip is

$$\Delta\Phi_{DIP} = \tan^{-1}\left(\frac{\omega_o M^2}{L_a R}\right) \qquad \text{Eq 1}$$

which is a measure of signal strength.

The industry is realizing the importance of thick resist processing in the semiconductor and MEMS market and thus many companies are recently competing to develop thick resist materials. Until now AZ4620 has been the thick resist used in this project to define molds for electroplating thick materials as in the case of the FINESS chip coils and NiFe ferrite cores. Two positive photo-resist materials have been studied, PLP100XT and AZ9260. PLP100XT is a new experimental positive resist. We have been able to spin a uniform 65μm thick layer of this resist; however, exposing and developing the resist has proven to be difficult due to over exposure/development of the sidewall profile. In contrast, promising results have been obtained using AZ9260 resist. A 30μm process has been developed and used for fabricating FI-HMS devices. Thus far we have been able to define ~30μm high structure with an 8μm line-width giving an aspect ratio of ≈4, although, according to literature this resist is capable of thicker structures [13]. A surface scanned profile of the patterned 30μm resist is shown in Figure 9. The Zygo software does not allow leveling of the 3D plot thus unfortunately a slope across the 2D plane is seen.

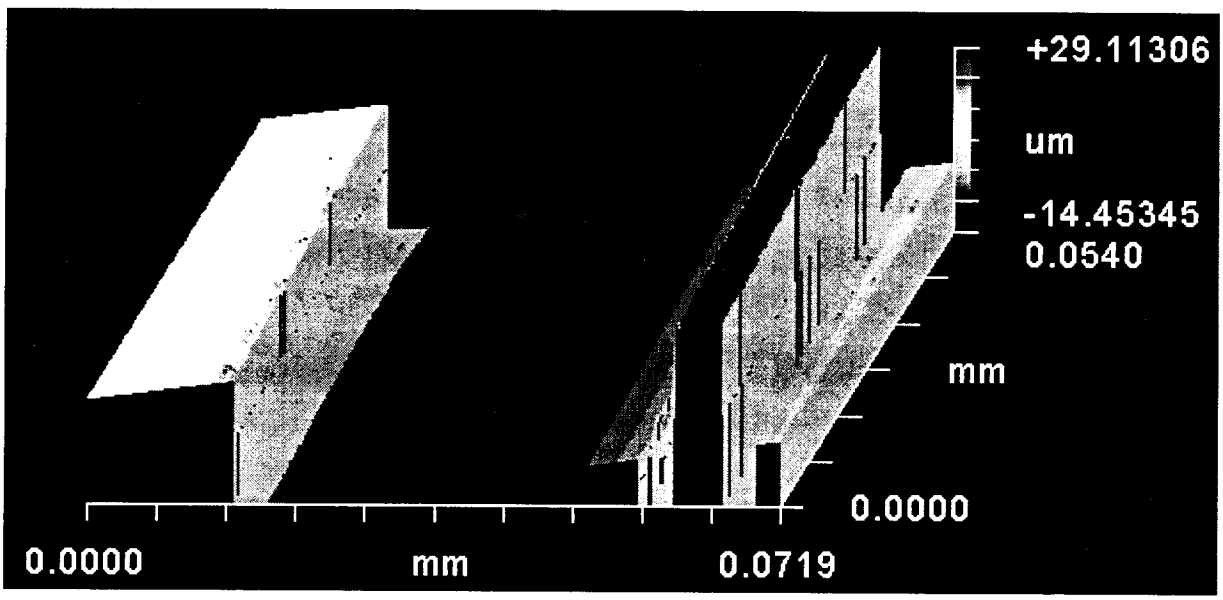


Figure 9: Zygo surface scan of AZ9260 30μm patterned resist.

The 30μm resist process is used to fabricate 30μm thick copper plated coils. An SEM and 3D surface profile scan is shown in Figures 10 & 11. Note that the copper coil is electroplated using the new process described in the next section.

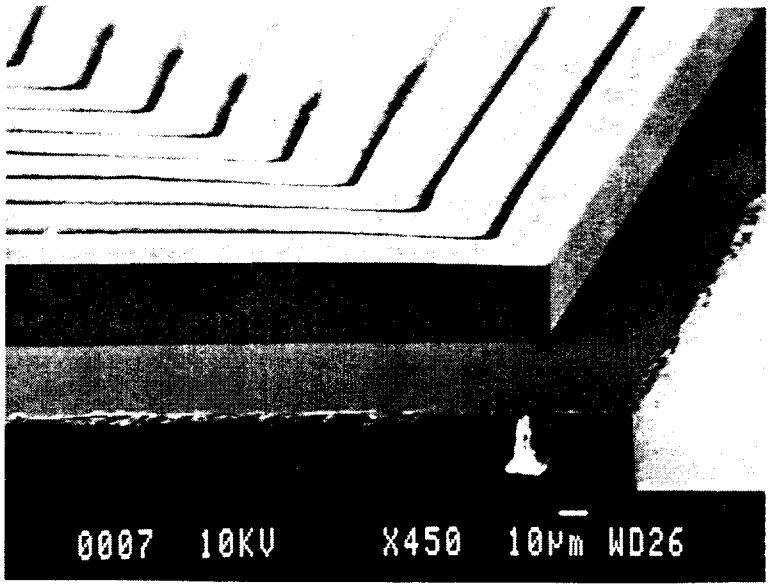


Figure 10: SEM of 30μm thick copper plated coil.

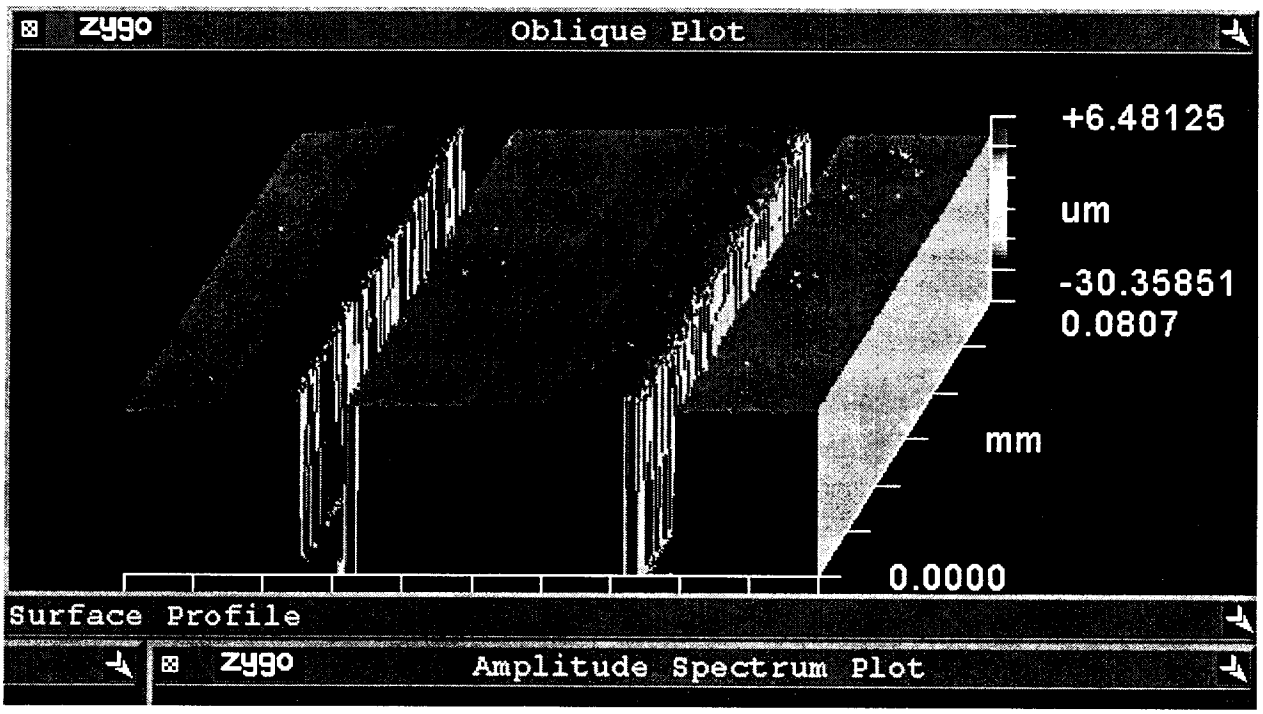


Figure 11: Zygo surface scan of 30μm thick copper plated coil.

We will attempt to obtain thicker resist molds with AZ9260 and also pursue other thick resist materials as they become available.

2.3.2 Advancements in Copper Electroplating

A vast improvement in the quality and plating rate has been realized with a new plating solution [13]. The new plating solution is compared to the old solution in Table 5.

Table 5: Electroplating solution

Old Plating Process:	New Plating Process:
Chemical List: DI H_2O Cupric Sulfate Sulfuric Acid	Chemical List: DI H_2O Cupric Sulfate Sulfuric Acid Hydrochloric Acid CUMAC additives
Surface uniformity: > ± 5μm Plating rate: ~ 2μm/hr Resistivity: > $3.2\times10^{-7}\Omega$cm	Surface uniformity: < ± 2μm Plating rate: ~ 0.5μm/min Resistivity: ~ $2.4\times10^{-7}\Omega$cm

As shown in Table 5, the new electroplating process shows improvements in surface uniformity, plating rate, and resistivity. Each of these characteristics contributes significantly to the quality of the fabricated coils. Increased surface uniformity allows one to plate the full thickness of the resist mold without being limited by spotted over-plating which can short adjacent features as shown in Figure 12 by a coil electroplated with the old plating process. For comparison a coil fabricated using the new electroplating solution is shown in Figure 13.

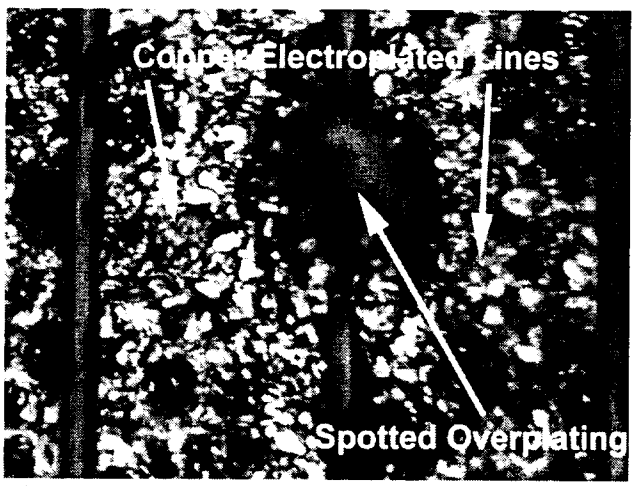


Figure 12: Spotted over-plating – common with old plating process (~18μm thick).

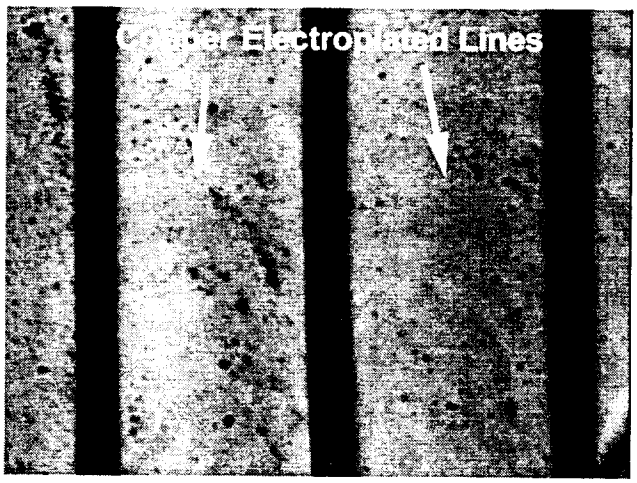


Figure 13: Uniform electroplating using new solution (20μm thick).

The improved plating rate increases throughput of devices. Considering that the old electroplating process took 10 hours of plating time to plate one wafer with 20μm of copper, it would not be feasible to use the same process for thicker plating. Therefore, the new electroplating process has made the FI-HMS fabrication process much less time consuming. Also, the new process has significantly lower resistivity than the old process, and thus the Q of the coils is inherently increased. Figures 14,15,16 and 17 show surface profile plots and SEM photographs of coils plated using the old and new plating processes.

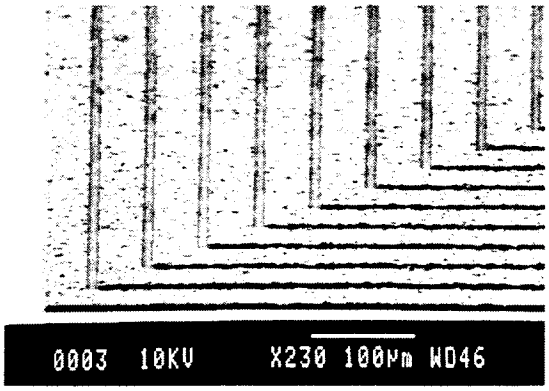


Figure 14: SEM of 15μm thick coil plated using the old process.

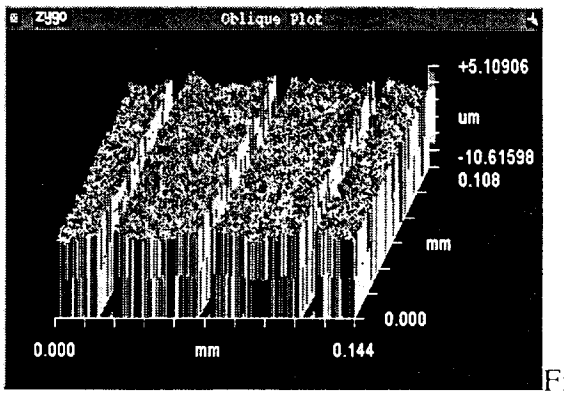


Figure 15: Zygo surface profile of 15μm thick coil plated using the old process.

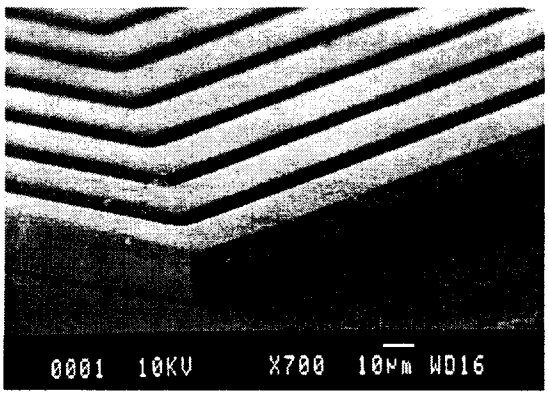


Figure 16: SEM of 20μm thick coil plated using the new process.

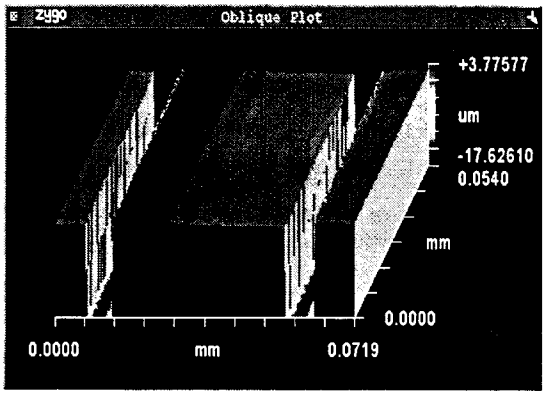


Figure 17: Zygo surface profile of 20μm thick coil plated using the new process.

Although the plating uniformity is very good locally the plating rate across the entire wafer varies as much as 5μm/hr. In order to obtain uniformity across the wafer a station dedicated for copper electroplating is being constructed. If plating non-uniformity becomes an issue other plating techniques such as pulsed current sources or various types of copper metal sources can be employed.

2.3.3 FI-HMS Model

In order to aid the development of the FI-HMS, expressions for inductance, series resistance, and capacitance are analyzed. The inductance expression has been previously reported with the design of the FINESS chip integrated planar copper coil inductor; whereas, the resistance and capacitance are obtained using the linear length of the entire coil, d_L. The expressions for L [10], R, and C are

$$k1 = L_{eff} \cdot \ln\left(L_{eff} + \sqrt{L_{eff}^{\ 2} + W_{eff}^{\ 2}}\right) \qquad \text{Eq. 2}$$

$$k2 = W_{eff} \cdot \ln\left(W_{eff} + \sqrt{L_{eff}^{\ 2} + W_{eff}^{\ 2}}\right) \qquad \text{Eq. 3}$$

$$L = 9.21\times10^{-9} \cdot N^2 \cdot \mu\left[\left(L_{eff} + W_{eff}\right) \cdot \ln\left(\frac{8 \cdot L_{eff} \cdot W_{eff}}{N \cdot h + N \cdot w}\right) - k1 - k2\right] \qquad \text{Eq. 4}$$

$$d_L = 2 \cdot N \cdot \left[\left(L_{coil} + W_{coil}\right) - 2 \cdot w - 2 \cdot (w + s) \cdot (N - 1)\right] \qquad \text{Eq. 5}$$

$$R = d_L \cdot \frac{\rho}{w \cdot h} \qquad \text{Eq. 6}$$

$$C_{substrate} = d_L \cdot \frac{w \cdot \varepsilon}{t} \qquad \text{Eq. 7}$$

Note that $C_{substrate}$ is not the total capacitance of the LC tank circuit and will be discussed in the next section. The equation nomenclature is provided in Table 6.

Table 6: Equation nomenclature for the FI-HMS.

FI-HMS:	
L_{coil}	length of the coil
W_{coil}	width of the coil
L_{eff}	effective length of the coil
W_{eff}	effective width of the coil
N	number of turns
h	coil height (plating height)
w	width of coil lines
s	spacing between adjacent coils
d_L	mutual inductance
t	dielectric thickness
ρ	resistivity
μ	permeability
ε	permittivity

These equations are used to evaluate experimental data presented in the next section.

2.3.4 FI-HMS Evaluation

The resistance, inductance, and resonant frequency of many FI-HMS devices with six different coil designs are measured. The six different device designs each $8\times1.5mm^2$ are listed in Table 7 and the R, L, and f_0 results are shown in Figures 18-20.

Table 7: FI-HMS Designs

Design	w	s	N
A	40	8	14
B	40	10	14
C	40	12	13
D	30	8	18
E	30	10	17
F	20	10	23

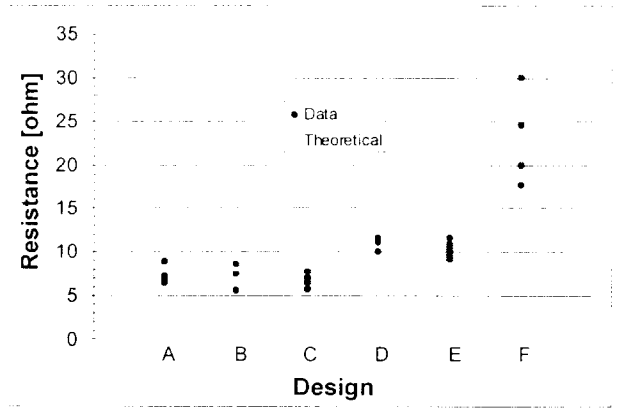


Figure 18: FI-HMS resistance.

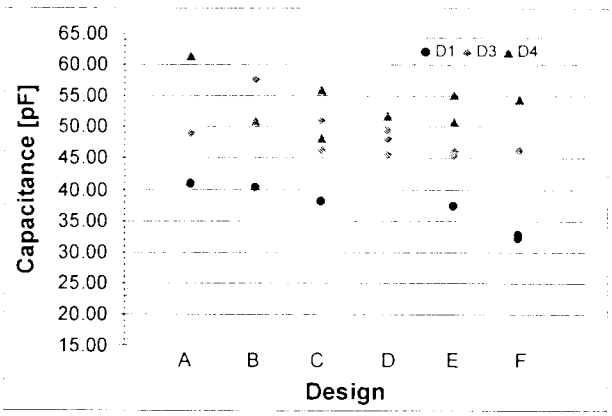


Figure 19: FI-HMS inductance

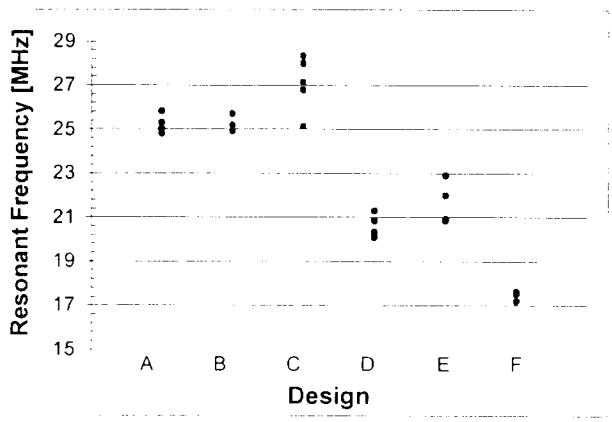


Figure 20: FI-HMS resonant frequency (constant %RH).

The experimental resistance data matches well with that derived from Eq 5. However, the measured inductance is roughly half of the predicted values using Eq 3. Thus a different inductance model is needed to compensate for the error.

In the coil model for FINESS copper plated coils it was stated that the dominant capacitance of the system was the substrate capacitance, $C_{subtrate}$, and that the coil capacitance was negligible [10]. However as the plating thickness increases and the dielectric thickness decreases the effect of the coil capacitance, C_{coil}, increases. Therefore, a new model for the FI-HMS capacitance must also be derived. This has yet to be accomplished however much can be learned from the data shown above in Figures 18, 19 and 20.

The experimental total FI-HMS capacitance is derived from the equation

$$f_o = \frac{1}{2\pi\sqrt{LC}} \quad \Rightarrow \quad C = \frac{1}{L\cdot(2\pi f_o)^2}. \qquad \text{Eq. 8}$$

The model for the FI-HMS system must account for the coil capacitance especially if coil thickness is to be increased for lower resistance coils. Figure 21 plots the total FI-HMS capacitance, C, calculated from the data using Eq. 7 and Figure 22 plots the theoretical substrate capacitance, $C_{substrate}$, calculated using Eq. 6.

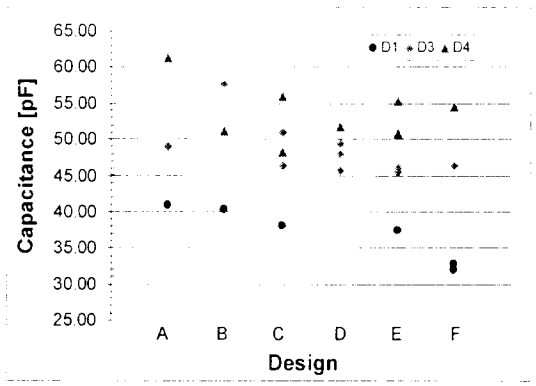


Figure 21: Calculated FI-HMS capacitance from measure L and f_o.

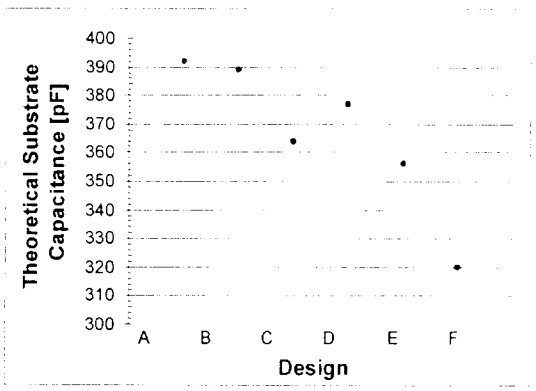


Figure 22: Theoretical Substrate Capacitance.

Notice the great difference between the calculated capacitances which strongly suggests that C_{coil} is not negligible in these devices.

2.3.4 FI-HMS Humidity Monitoring Results

Three FI-HMS devices with 20μm electroplated copper are calibrated in the humidity chamber. Calibration data is shown in Figures 23 & 24.

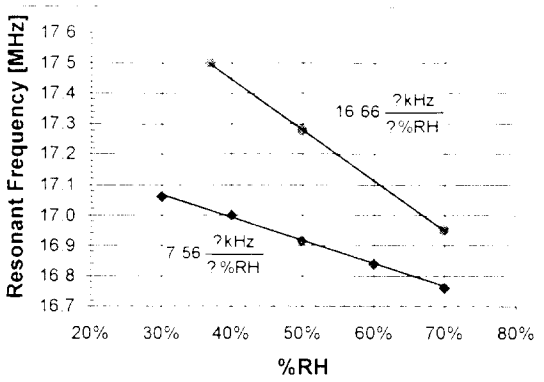


Figure 23: Calibration data of two FI-HMS devices (both design F).

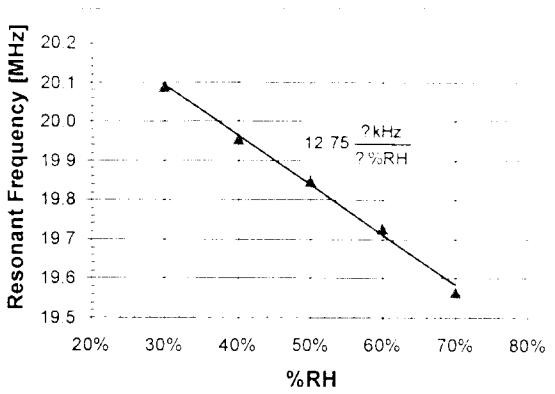


Figure 24: Calibration of FI-HMS device (design D).

Figure 25 shows the frequency response curve of the data shown in Figure 24.

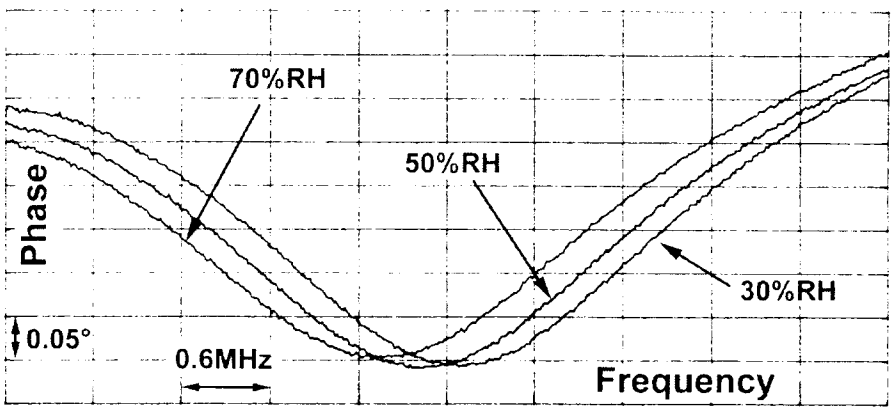


Figure 25: Frequency response curve of calibrated device.

It is not understood at this time why the devices show sensitivity variances of 16.6kHz per %RH, 12.75kHz per %RH, and 7.56kHz per %RH. These results show that humidity can be monitored using FI-HMS devices described here.

2.4 In-Vivo Testing

With the development of the wireless humidity monitoring system, it is possible to remotely monitor package integrity while the device is implanted in an animal host. Consequently, six devices were prepared and screened to insure hermetic seals. Each device passed a one-day room temperature soak in DI water to validate the seal prior to implant. The devices were then sent to the University of Michigan Medical School for implantation into guinea pig hosts. Two guinea pigs have been implanted with packages to monitor hermeticity in the in-vivo environment. Sites on the guinea pigs were selected to give the widest possible range of environmental conditions. On each host, one package was implanted into the leg, another into the abdomen, and a final one into the head for a total of

three packages per host. Devices were implanted in the head beneath the skull but above the dura, under the skin on top of the leg muscle, and in the abdominal cavity as depicted in Figure 26.

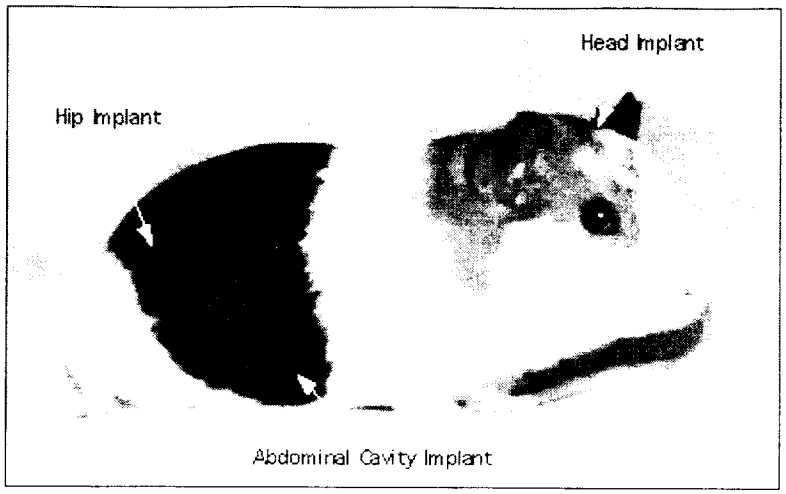


Figure 26: Locations of implanted packages in guinea pig host.

Tests were conducted immediately prior to and following implant, with no discernible change in system output. After this, devices were measured biweekly to detect shifts in resonant frequency resulting from changes of humidity in the package if any. As of April 4, 2000 there has been no discernible shift in the output of any humidity sensing systems inside the packages. Given that a 50 kHz shift is considered significant, the output of the sensors, which varies by only a few kilohertz, indicates fairly steady humidity inside the packages. Figures 27 and 28 show the measured frequencies of the sensors over the duration of the test.

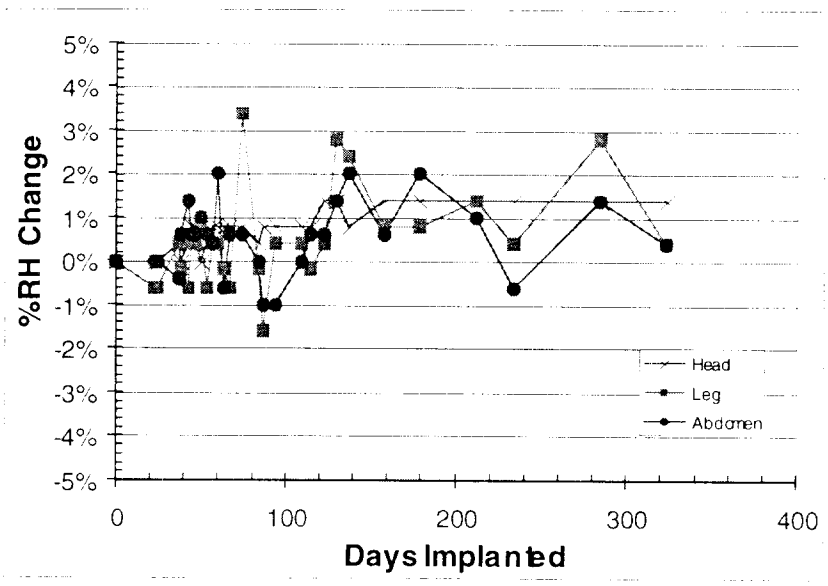


Figure 27: %RH change measurements over time for Guinea Pig A.

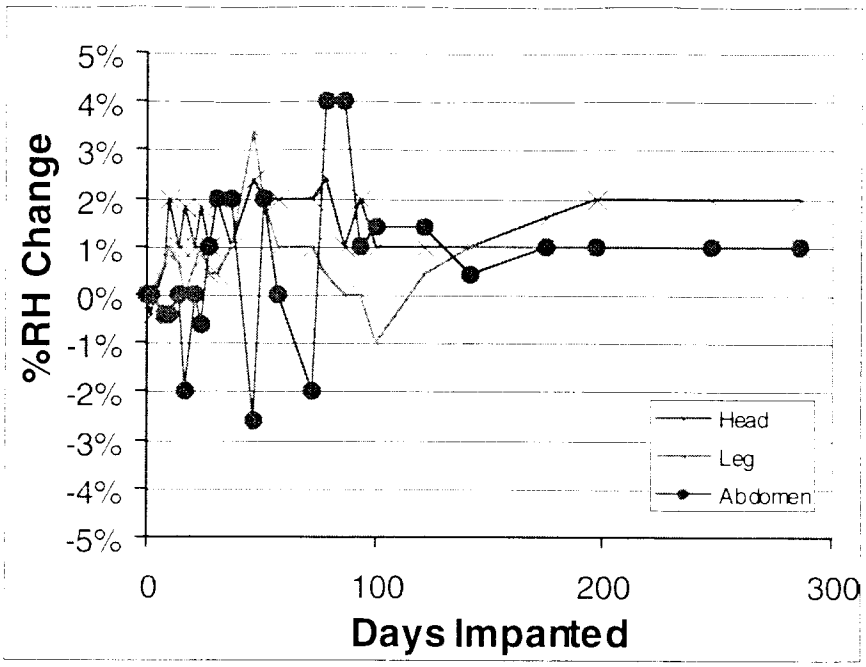


Figure 28: %RH change measurements over time for Guinea Pig B.

We will continue testing the packages in the guinea pigs biweekly and will report further data as it becomes available in the next quarter. The main goal from these tests is to demonstrate that these packages can stay hermetic inside animal hosts.

2.5 Novel Packaging Technologies

In the interest of developing a Si-Si bonding technology for flip chip devices, several novel encapsulation techniques have been investigated. The goal of this research is to find a technology that is biocompatible and can be used to make complicated bioMEMS systems. Current microsystems designed for biological applications are limited by low yield resulting from complicated process flows. By developing a technology that can separate the complexities of circuit design from the complexities of building implantable microsystems, it is possible to greatly simplify the production of implantable biosystems. Critical to this research is to develop a method that makes low temperature hermetic biocompatible encapsulation possible for Si-Si bonding. The long-term goal of this research is to enable the production of devices that are structurally similar to Figure 29.

2.5.1 Localized Heating

Initially developed by Motorola for bonding substrates together, localized heating technology has been adopted by Michigan researchers for use in a variety of applications. This technology uses polysilicon resistive heaters to create a localized heating region. The polysilicon is heated to a temperature that is often substantially higher than the thermal budget of the chip. Since the heating is extremely localized, the chip never exceeds its maximum allowable temperature and the chip's operation is not impinged. This allows the

formation of high temperature bonds on chips containing active circuitry. Cheng [3] has previously reported that it is possible to create fusion bonds in excess of 1000 °C, while having no noticeable temperature gain as close as 15 μm to the bond ring. As such, this technology has obvious applications in the biopackaging field. To explore this technology, a test structure has been designed and fabricated. The process used to build this test structure is outlined in Figure 30.

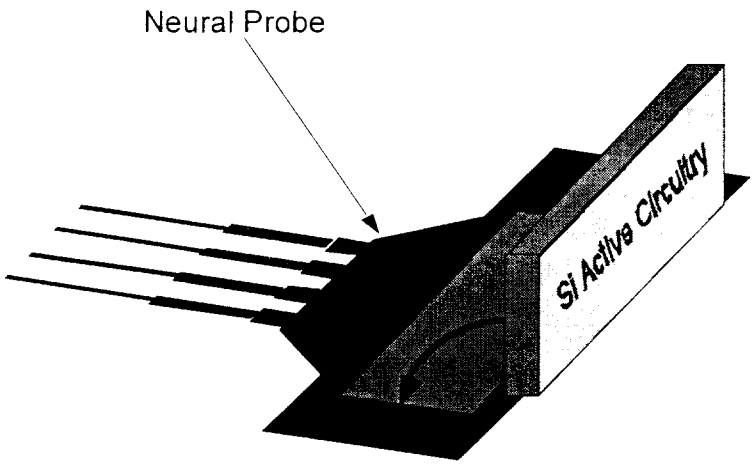


Figure 29: Long-term plan for flip chip technology.

This technology can be used to bond multiple material combinations. Since biocompatible devices have a limited number of available materials, there are only a limited number of bonds that can be reasonably made. There are three principle bonds that will be investigated: Si/Au Eutectic, Au/Au melt bond, and Ti/Si_3N_4 bonding. The eutectic bond has been developed using more conventional global heating techniques. It is well known that a Si/Au material stack will form an 18% Si eutectic at 363°C. This eutectic, which is similar in many ways to solder, can flow over step heights and should be able to create a planar bond. While few researchers have been able to report hermetic eutectic bonds, we hope to overcome this hurdle by using higher temperatures than normally available (~450°C) and by using multiple heating steps to create a more uniform eutectic. The Au/Au melt bond is a bond that can only be made via localized heating. The concept here is relatively simple. It is well known that gold will melt above 1063 °C. By bringing two gold layers into intimate contact and heating them to above 1063 °C, it should be possible to melt the two layers together and form a uniform bond. The third technology that will be researched is titanium nitridization. It has been reported that titanium will bond to silicon nitride at high temperature. By heating up a titanium layer, it should be possible to create a titanium nitride bond. Since titanium is an established biocompatible material, there is no reason to expect that this bond will not be biocompatible as well.

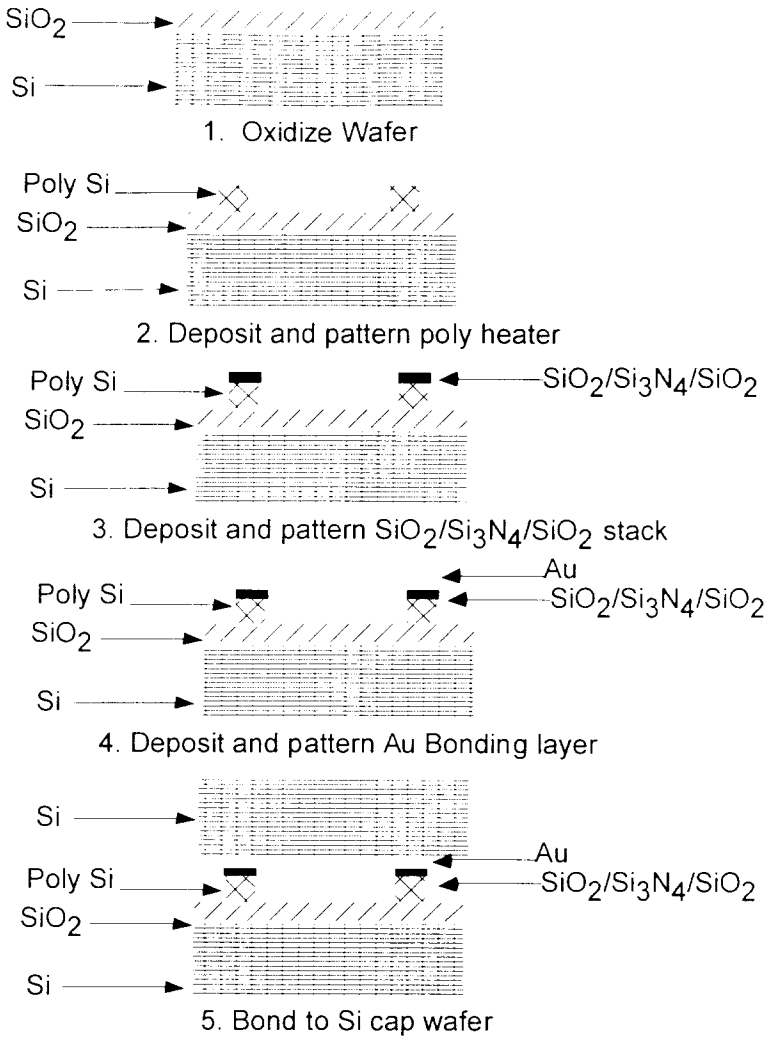


Figure 30: Process Flow for Localized Eutectic Bonding.

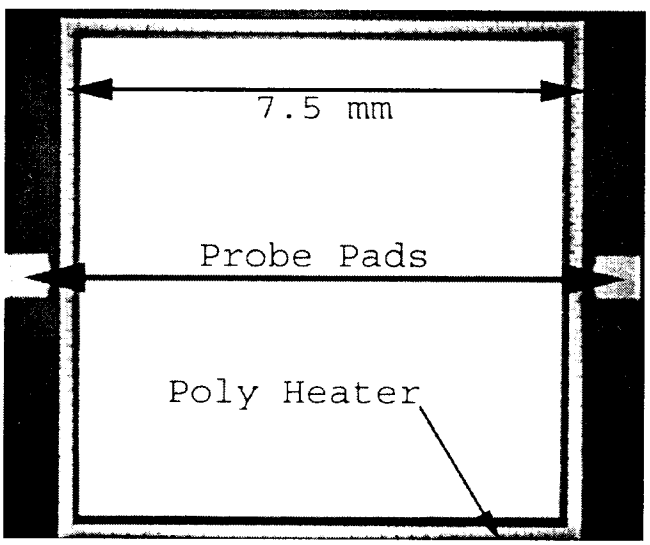


Figure 31: Test Structure for localized heating.

In the past quarter, a localized bonding test structure was tested. This structure, shown in Figure 31, has a 7.5mm long bondring with notches cut into it to simulate the step height caused by feedthroughs. This device size was chosen to simulate the bond area of the largest devices made at the University of Michigan. Using the test station depicted in Figure 32, the devices were tested under DC and pulsed power to achieve localized heating.

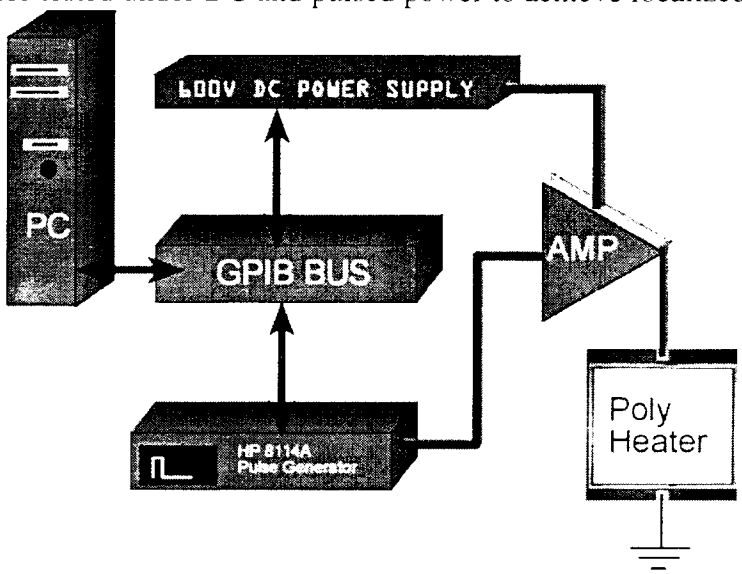


Figure 32: Computerized Control for Localized Bonding

To measure device temperature, a resistance versus power plot was generated, which is shown in Figure 33. Since change in resistance is proportional to temperature, a resistance plot versus a calibrated resistance measurement reveals temperature. The plot shows that the polyheater is not reaching the critical eutectic temperature of 363 °C. Before this temperature is reached, the current will breakthrough the protective dielectrics and flow through the lower resistance gold layer. This discovery lead to development of a new bonding technology. By rapidly inducing dielectric breakdown, it is possible to create a micro-arc weld. This weld is similar to conventional macro scale welding in that it uses a high electron flow to locally melt two layers together. The micro arc welding technology showed some promising results, as shown in Figures 34 and 35.

However, while the arc welding process creates strong die attach bonds, it is unlikely to produce reliable hermetic seals. As such, the localized heating structures were redesigned for improved thermal conduction and higher maximum temperature. Using the failure mechanisms discovered in this first test structure, it is possible to make a working test structure that should meet all of the project requirements.

Using the thermal conduction models developed from the first test structure, a second test structure was designed and fabricated. This test structure used 24 parallel heaters to limit the power dissipation over the whole die and to improve reliability of the packaging process. Temperature versus applied power was modeled to determine the device parameters for this second structure.

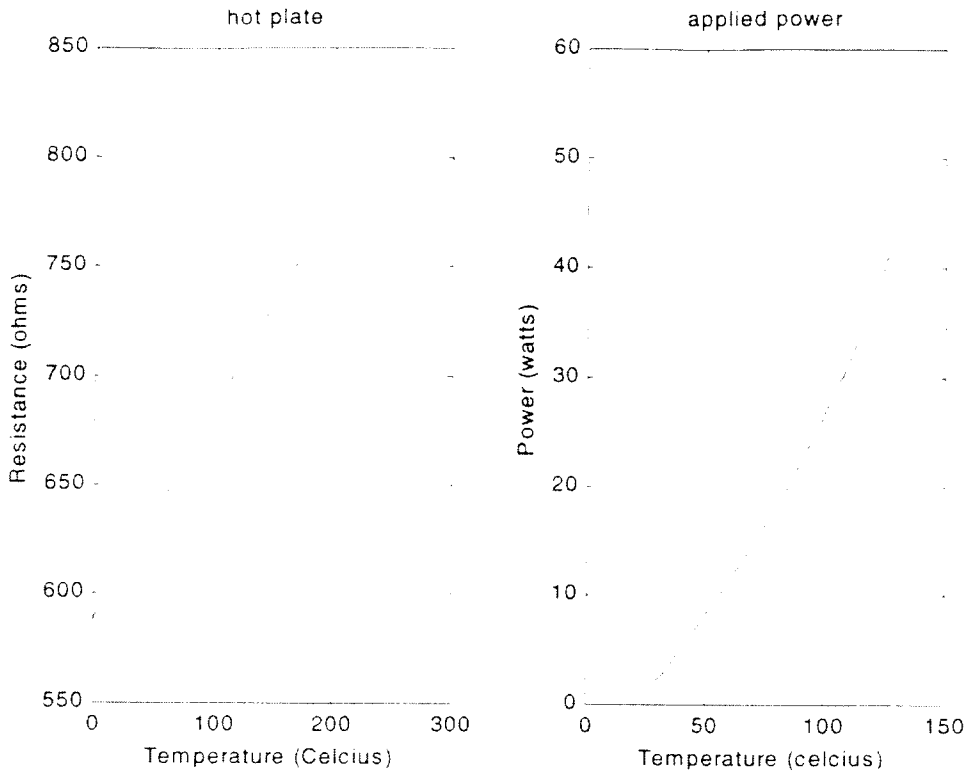


Figure 33: Temperature Curve for Localized Bonding

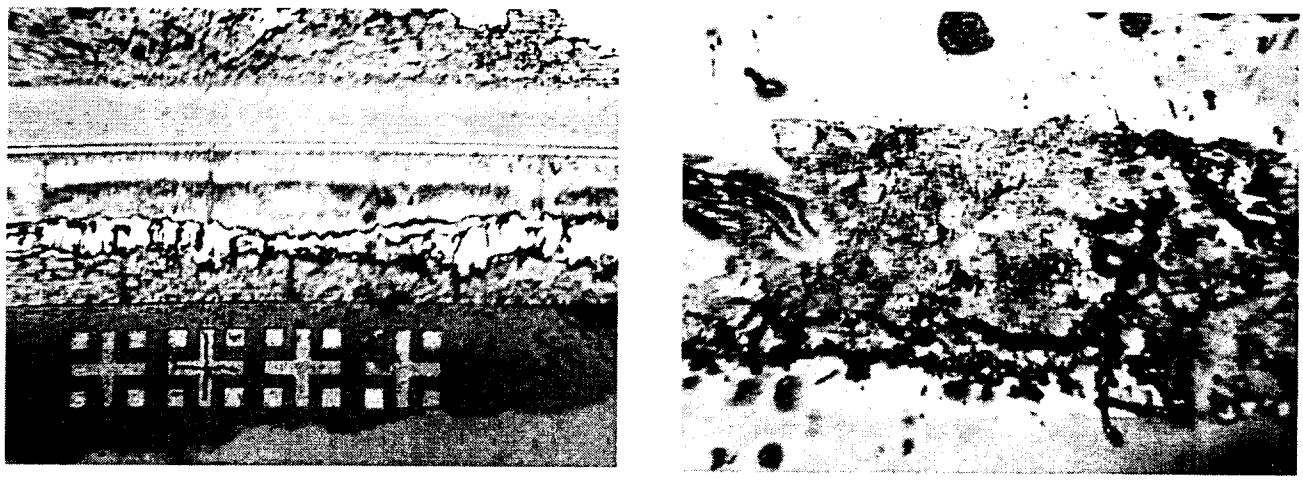


Figure 34: Picture of micro arc welding showing poly heater on the left and titanium coated Si cap wafer on right.

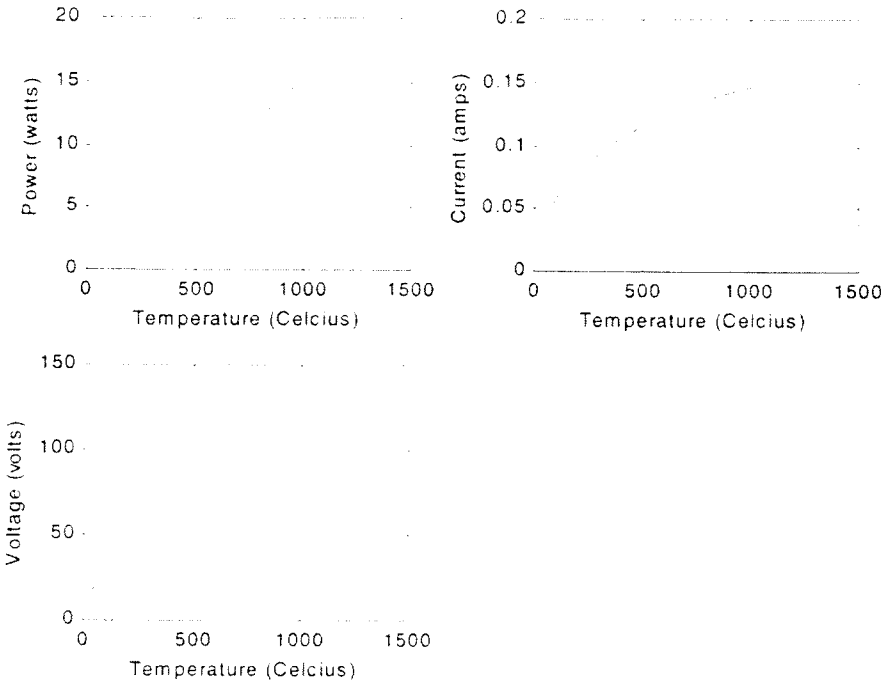


Figure 35: Modeling for second localized heating test structure.

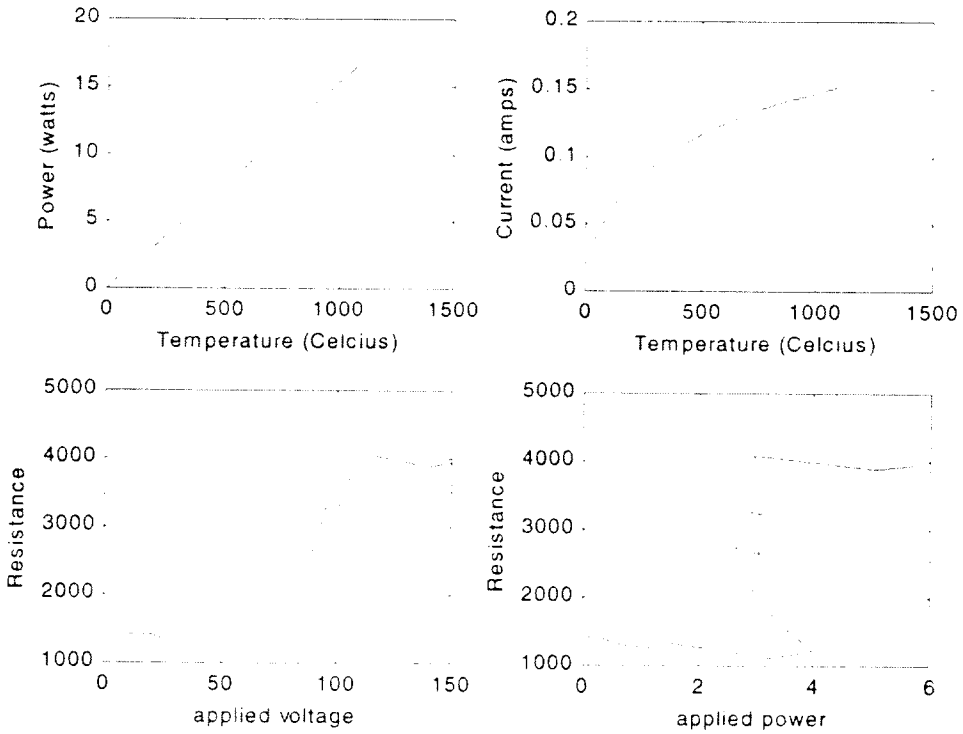


Figure 36: Measured temperature and resistance curves for the new localized heating structure (bottom) and theory (top).

As can be seen, this structure uses a smaller power load to achieve the temperature requirements of the first device. In this structure only 15 W is required to achieve the same temperature that the first test structure would have reached with 300 W. This structure was tested and the Voltage vs. Resistance plot is shown in Figure 36.

As this plot demonstrates, there is a sharp increase in resistance with voltage at 60V DC. This is a function of semiconductor physics that did not show up in the other samples due to the fact that they were degenerately doped. From theory, this transition point should occur around 500 °C, which would indicate that the new structures are reaching the required eutectic temperature. In the coming quarter we plan to demonstrate the efficacy of this new structure and create eutectic bonds.

In order to control the conditions of heating for localized bonding, computer programs were developed to manage the bonding process. Using LabVIEW and the setup depicted in Figure 32, these programs control the HP 8114A pulse generator and a 600V power source so that the electrical power supplied to the localized heaters can be ramped. This program controls the pulse width, which is related to the heating selectivity as well as annealing voltages and ramping times. This will provide the ability to slowly anneal the bonds, which should create better uniformity. The interface for this annealed heating is shown in Figure 37.

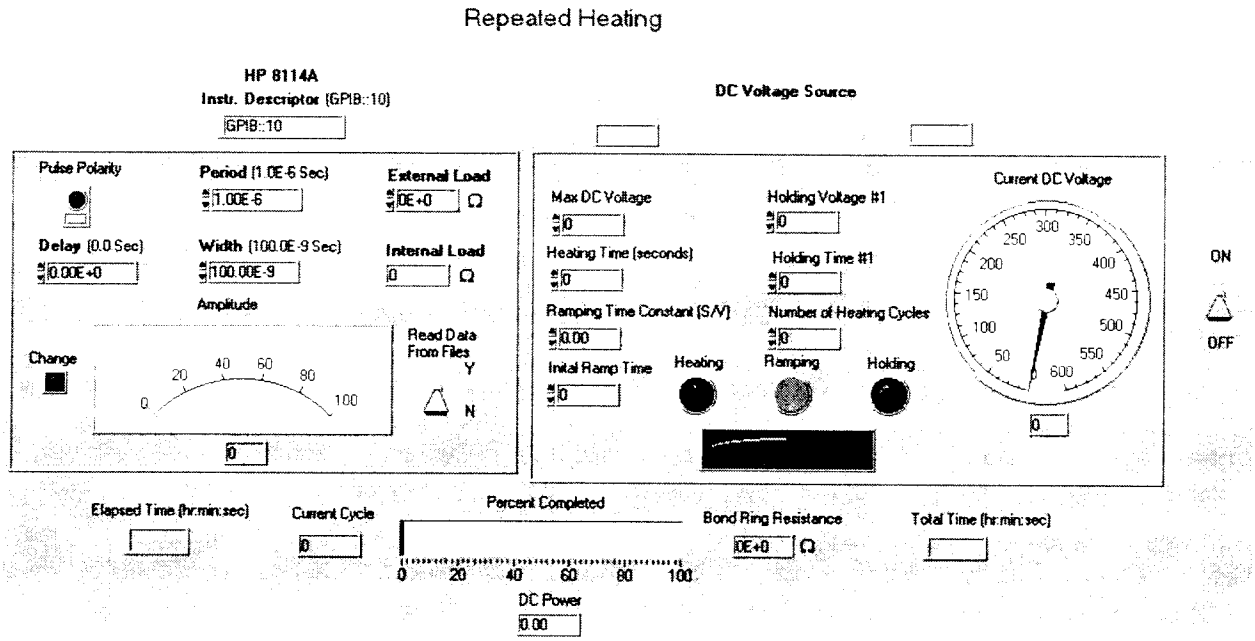


Figure 37: LabVIEW Program to Control Localized Heating

2.6 Testing of the FINESS chip-Class E transmitter system

This quarter, we tested the integrated coils with the transmitter. The transmitted power was found to be inadequate for the integrated coil to receive the essential 15mW of power for the FINESS chip [10]. To get more power output, we changed the components of the transmitter. Figure 38 shows the transmitter [14].

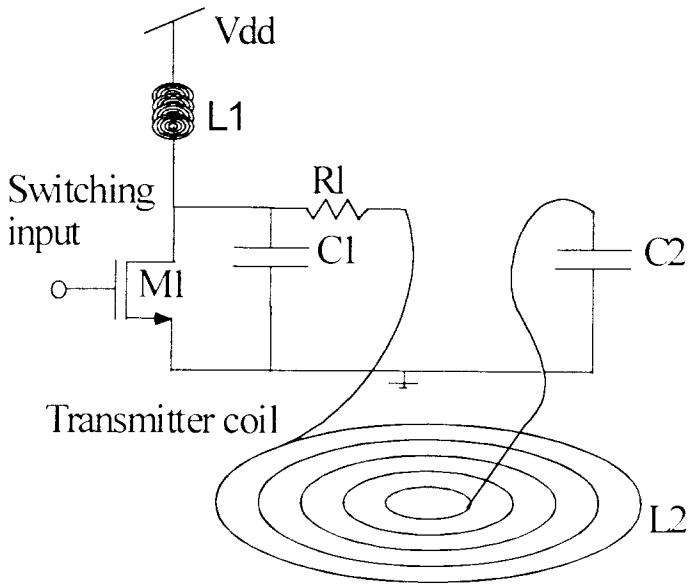


Figure 38: The Class E transmitter

Tables 8 and 9 show the components and the performance of the new Class E transmitter

Table 8: Component values for the Class E transmitter

L1	25μH
L2	55.4μH
C1	100pF
C2	30pF
Rl	5Ω

Table 9: Important measured performance characteristics of the self-oscillating Class E transmitter.

Parameter	*Value*
Nominal Frequency (fo)	4.09MHz
Efficiency at normal frequency	53.8%
Supply voltage and Current	18V, 130mA

We also derived a new set of equations for calculation of the power transferred with the telemetry link. The only modification made in this theory from the earlier one is the equation for the calculation of the mutual inductance for the telemetry link.

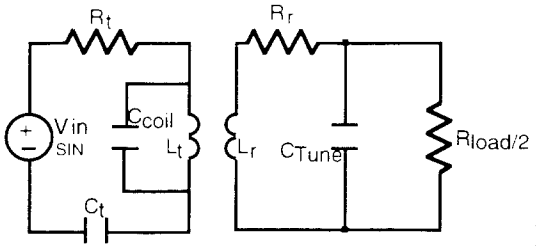


Figure 39: The equivalent circuitry of the telemetry link.

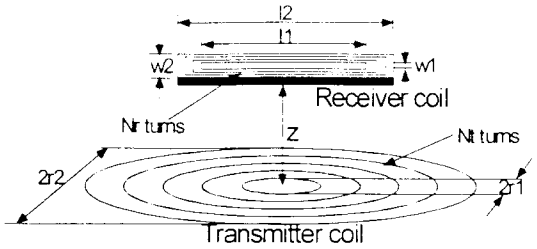


Figure 40: Illustrating the dimensions of the telemetry link

For the telemetry link equivalent circuitry illustrated in figure 39 with the dimensions as given in figure 40, the equations are:

$$M = \sum_{m=0}^{N_r-1}\left(L_1 + \frac{L_2 - L_1}{N_r - 1}.m\right)\left(W_1 + \frac{W_2 - W_1}{N_r - 1}.m\right)\frac{\mu_0}{2}\sqrt{\mu_{core}}\sum_{k=0}^{N_t-1}\frac{\left(r_1 + \frac{r_2 - r_1}{N_t - 1}.k\right)^2}{\left\{\left(r_1 + \frac{r_2 - r_1}{N_t - 1}.k\right)^2 + z^2\right\}^{3/2}} \quad \text{Eq. 9}$$

$$|I_r| = \frac{\left(|I_t|\cdot\omega M\right)}{\sqrt{\left(R_r + \frac{2R_{load}}{4 + \omega^2 C_{tune}^2 R_{load}^2}\right)^2 + \left(\omega L_r - \frac{\omega C_{tune} R_{load}^2}{4 + \omega^2 C_{tune}^2 R_{load}^2}\right)^2}} \quad \text{Eq. 10}$$

$$|V_{load}| = |I_r|\sqrt{\left(\frac{2R_{load}}{4 + \omega^2 C_{tune}^2 R_{load}^2}\right)^2 + \left(\frac{\omega C_{tune} R_{load}^2}{4 + \omega^2 C_{tune}^2 R_{load}^2}\right)^2} \quad \text{Eq. 11}$$

$$P_{received} = \frac{1}{2}\cdot\frac{|V_{load}|^2}{R_{load}/2} \quad \text{Eq. 12}$$

The results on application of these equations agree closely with the obtained values of received powers with distance from the transmitter axis, as seen from figure 41. It can also be seen in the figure that the required power of 15mW is easily reached when the receiver coil is about 1 cm from the transmitter coil.

We also hope that the new coils being fabricated for the humidity sensors (described in sections 2.3.1 and 2.3.2)can be incorporated into the FINESS chip. If that is done, theory indicates that the received power can be doubled, as shown in figure 42.

Table 10: Equation nomenclature for the power transfer in the FINESS system

M	Mutual inductance	C_{tune}	Tuning capacitor in parallel with receiver coil
μ_{core}	relative permeability of the NiFe core	L_r	Receiver coil inductance
μ_0	absolute permeability of free space	V_{load}	Voltage across load resistance
N_r	Turns in the receiver coil	$P_{received}$	Received power across load
N_t	Turns of the transmitter coil	L_1	smallest length of the receiver coil
I_r	Current in receiver coil	L_2	largest length of the receiver coil
I_t	Current in transmitter coil	W_1	smallest width of the receiver coil
ω	Frequency of transmitted signal	W_2	largest width of the receiver coil
R_r	Receiver coil resistance	r_1	the radius of the innermost turn in the transmitter coil
R_{load}	Load resistance	r_2	the radius of the outermost turn in the transmitter coil
m , k	Indices for summation	z	distance of the receiver from transmitter plane

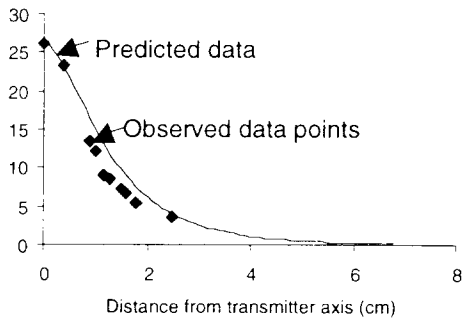


Figure 41: Received power vs. distance of receiver coil from transmitter

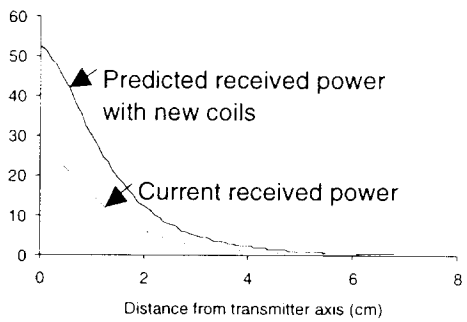


Figure 42: Predicted values of received power with new coils

III. PLANS FOR THE COMING QUARTER

Further research into thick resist materials and process for increased plating height will continue. FI-HMS devices will be characterized and an accurate model will be developed so that the design can be optimized for sensitivity, testing distance. After testing and characterization of the FI-HMS devices they may be used for humidity monitoring in the glass silicon package. We will continue wireless monitoring the of the implanted packages.

Research will be continued in the area of silicon to silicon flip chip packages. The localized heating work will be concluded and other technologies will be researched. A demonstration of these technologies onto a neural probe substrate will also be attempted to demonstrate the viability of these new packaging technology.

Testing of FINESS chips with modulated signals from the transmitter will begin this quarter. We will use the new techniques developed for electroplating coils to plate inductors for the FINESS chip. We will work closely with our collaborators for testing these chips *in vivo*.

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